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PATENT, TRADEMARK, COPYRIGHT AND RELATED CAUSES

November 2, 2004

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Re: U.S. Patent Application for:
"MULTI-CHIP MODULE"
Serial No. 09/936962; Filed December 27, 2001
Patent No. 6788546; Issued September 7, 2004
First Named Inventor: Philippe Steiert et al.
Our Reference No. FRR-12671

Dear Sir/Madam:

A Certificate of Correction under 35 U.S.C. 254 is hereby requested to correct Patent Office printing errors in the above-identified patent. Enclosed herewith is a proposed Certificate of Correction (Form No. PTO/SB/44) for consideration.

It is requested that the Certificate of Correction be completed and mailed at an early date to the undersigned attorney of record. The proposed corrections are obvious ones and do not in any way change the sense of the application.

We understand that a check is not required since the errors were on the part of the Patent and Trademark Office in printing the patent.

Very truly yours,

David E. Spaw, Reg. No. 34732

DES:ps
Enclosure

PTO/SB/44 (07-03)
Approved for use through 01/31/2004. OMB 0651-0033
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.
(Also Form PTO-1050)

UNITED STATES PATENT AND TRADEMARK OFFICE
CERTIFICATE OF CORRECTION

PATENT NO. : 6,788,546 B1
DATED : September 7, 2004
INVENTOR(S) : Phillipe Steiert et al.

It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

Title Page:
Replace entire abstract with the following abstract:

--A multi-chip-module includes a base carrier on which signal conductor tracks and signal contact surfaces arranged at least in a single layer are located, and with a semiconductor component operating in the signal range and connected with the signal conductor track and signal contact surfaces. A high degree of integration is achieved with a multi-chip-module of this type. In some areas on the base carrier power conductor tracks and power contact surfaces arranged in at least one layer are located. Furthermore, at least one power electronics component, operating in the power range, is provided, which is connected with at least one power conductor track, at least one power contact surface and at least one signal conductor track. The power conductor tracks have a larger cross section than the signal conductor tracks at least on the basis of greater thickness dimensions.--

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PATENT NO. 6,788,546

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